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Annual Progress Report

for

Design and Packaging of Fault Tolerant Optoelectronic Multiprocessor Computing System

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The goals for the project are primarily to develop the packaging technology, by integrating silicon CMOS chips, detectors, modulators, diffractive optical elements and/or photorefractive nonlinear crystals in packaging design and to assemble packaged fault tolerant systems using the developed technologies. On the secondary basis, we would model package systems and establish a data-base for CAD, and investigate the design of fault tolerant optoelectronic system. Our accomplishments for the period from December 14, 1992 to December 14, 1993 are summarized below.

(1) Developed packaging technologies for self-alignment based on flip-chip bonding and in-situ holograms recording. Developed and fabricated optoelectronic components useful for system packaging.

(1a) Developed alignment analysis in packaging of free space optoelectronic interconnect module. The analysis includes optical effect (e.g. wavelength shift), thermal effect (e.g. different expansion due to different materials), and mechanical effect (e.g. misalignment during assembly as well as misalignment due to component manufacturing tolerance). The results of analysis indicate that: (i) The misalignment due to optical effect has the least effect (< 1 μm). The misalignment due to thermal effect becomes important (about 7 μm) if an improper material combination is used; it can be reduced to less than 2 μm when an optimum material combination is chosen. The misalignment due to mechanical effect is most dominant (about 7 μm); however assembly tolerance can be reduced to less than 2 μm by using optimum flip-chip reflow process and optimum flip-chip bonding pads design along with the use of highly accurate Talbot-Moiré alignment technique (< 0.2μm) [1, 4-6]. (ii) The achievable initial alignment during assembly (such as flip-chip soldering) should be very tight for operation over larger temperature range. (iii) System with low f-number (smaller volume) and smaller detector size (higher processing speed) has generally more stringent alignment requirements. Details are provided in Appendix A and B.

(1b) To achieve consistent sub-micron self alignment using flip-chip bonding, a comprehensive physical model representing the flip-chip bonding reflow process is being developed and to be verified by experiments. Such a model includes a static model to optimize reflow joint design and a dynamic model to simulate the solder reflow process. Details are provided in Appendix A.

(1c) Developed Talbot-Moiré alignment technique for high accuracy (< 0.2 μm) alignment of substrates with separations from a few microns to a few centimeters. This technique is employed to assemble packages of multilayer structures. Details are provided in Appendix A.

(1d) Developed self-alignment technique using in-situ hologram recording in photorefractive crystals (PRCs). The technique also allows for reconfiguring the interconnect link via updating the interconnect holograms without requiring re-alignment [2,7]. Details are provided in Appendix C and D.

(1e) Polarization selective gratings were fabricated in photorefractive crystal (PRC) $LiNbO_3$ with an over all efficiency of 25% and contrast ratio of 70:1.

(1f) CGHs with diffraction efficiency higher than 90% for optical interconnect are fabricated by one step direct write electron beam on analog resists, which has the equivalent diffraction efficiency of a 8-level phase CGH [8-12]. Details are provided in Appendix E, F and G.

(1g) An 8x8 PLZT spatial light modulator is being assembled with lenslet arrays and polarizer in a ceramic packaging, which is immediate applicable to generic system packaging applications.

(2) Made progress toward assembling (packaging) two prototype systems

(2a) Designed a chip consisting of 4x4 switching elements for the prototype demonstration of a fault tolerant 4-stage interconnection network based on twin butterfly architecture. Developed substrate layout for a Si/PLZT based OE-MCM optical interconnection. Designed CGHs for routing of the free space optical channels. Components are being fabricated, and the system will be assembled and tested within next few months.

(2b) Designed physical layout for packaging of a general purpose reconfigurable interconnect module using PRC for applications such as matrix-matrix multiplication or neural network. This interconnect module, with input/output array size of 8x8, was designed to be able to demonstrate its self-alignment capability and reconfigurability. Components such as PLZT-SLMs for displaying input and interconnect weights and CGHs for imaging and Fourier transform are being fabricated, and the system will be assembled within the next few months.

(3) Developed simulation models for OE components and free space optical links

(3a) Components such as source/modulator, detectors, refractive/diffractive optical elements are modeled to be incorporated in the link model [13-14]. The link model will constitute the core of optoelectronic system optimization by simulation. the Details are provided in Appendix H and I.

(3b) The algorithms of placing processing elements (PEs) in an OE-MCM were incorporated in the system modeling. Applying this placement algorithm reduces the longest interconnect distance and increase the system size by 50% without exceeding the fabrication limits of computer holograms for optical interconnects[3, 15-16]. Details are provided in Appendix J.

(3c) The algorithms of partitioning OE multichip module for effective utilization of optical as well as electronic interconnection technologies were developed and incorporated into the system modeling. The application of this algorithm to a design example of multistage interconnection network of OE MCM showed a 50% reduction in power required for interconnects [17-18]. Details are provided in Appendix K.

REFERENCE

Refereed Publications

[1] S.K. Patra, J. Ma, V.H. Ozguz, and S.H. Lee, "Alignment issues in packaging for free space optical interconnects," _Optical Engineering_, accepted for publication. (see Appendix A)

[2] H. Takahashi, D. Zaleta, J. Ma, J.E. Ford, Y. Fainman, and S.H. Lee, "Packaged optical interconnection system based on photorefractive correlation," _Applied Optics_, accepted for publication. (see Appendix C)

[3] D. Zaleta, J. Fan, B.C. Kress, S.H. Lee, and C.K. Cheng, "Optimum placement for optoelectronic multichip modules and synthesis of diffractive optics for MCM interconnects," _Applied Optics_, accepted for publication. (see Appendix J)

Presentations in Conferences

[4] S.K. Patra, J. Ma, V.H. Ozguz, and S.H. Lee, "Self-alignment by flip-chip bonding for OE-MCM packaging" (Invited), _Proc. SPIE_, 2153, 1994 .

[5] S.K. Patra, J. Ma, and S.H. Lee, "Alignment issue relating to flip-chip bonding requirement for holographic optical interconnects," _ASEM International Electronics Packaging Conference_, Sept., 1993, Binghampton, N.Y..

[6] D. Zaleta, S.K. Patra, J. Ma, and S.H. Lee, "Misalignment sensitivity analysis of planar optical interconnect systems", _Proc. SPIE_, 2153, 1994. (see Appendix B)

[7] J. Ma, B. Catanzaro, W. Daschner, Y. Fainman, and S.H. Lee, "Packaged reconfigurable space-variant optical interconnect using wavelength multiplexed volume holograms," _Proc. SPIE_, 1849, 116-128(1993). (see Appendix D)

[8] D. Zaleta, W. Daschner, M. Larsson, B. Kress, J. Fan, K.S. Urquhart, and S.H. Lee, "Diffractive optics fabricated by electron-beam direct write methods," _Proc. SPIE_ Critical Review, CR49, 1993. (see Appendix E)

[9] S.H. Lee, "Diffractive optics and computer-generated holograms for optical interconnects," _Proc. SPIE_ Critical Review, CR49, 1993.

[10] S.H. Lee, "Diffractive optics fabricated by direct write with electron beam on analog resists," (Invited) _1993 OSA Annual Meeting_, Toronto (October 1993).

[11] J. Fan, D. Zaleta, and S.H. Lee, "An algorithm for the generation of reduced E-beam fabrication data for general aspheric diffractive optical elements," submitted to _OSA Topical Meeting on Diffractive Optics_, Rochester(June 1994). (see Appendix F)

[12] D. Zaleta, M. Larsson, W. Daschner, and S.H. Lee, "Coupled kinoforms to increase power throughput for space variant optical interconnect systems," submitted to _OSA Topical Meeting on Diffractive Optics_, Rochester (June 1994). (see Appendix G)

[13] S.H. Lee, V.H. Ozguz, J. Fan, D. Zaleta, and C.K. Cheng, "Computer aided design and packaging optoelectronic systems with free space optical interconnects", *IEEE 1993 Custom Integrated Circuits Conference*, May 9-12, 1993. (see Appendix H)

[14] D.-T. Lu, W.P. Poon, T.-T.Y. Lin, and S.H. Lee, "Optoelectronic component modeling and system simulation," *1993 OSA Annual Meeting* , Toronto(October 1993). (see Appendix I)

[15] J. Fan, D. Zaleta, C.K. Cheng, and S.H. Lee, "Physical layout for computer generated holograms for optoelectronic multichip modules", *IEEE MCM Conference*, 198-203(1993).

[16] D. Zaleta, J. Fan, C.K. Cheng, and S.H. Lee, "Simulated annealing applied to placement of processing elements in optoelectronic multichip modules interconnected by computer generated holograms", *OSA Topical Meeting on Optical Computing*, 196-199(1993).

[17] J. Fan, B. Catanzaro, V.H. Ozguz, C.K. Cheng, and S.H. Lee, "Design considerations and algorithms for partitioning opto-electronic multichip modules," *The First International Workshop on Massive parallel Processing using Optical Interconnections*, Cancun Mexico, April, 1994. (see Appendix K)

[18] J. Fan, B. Catanzaro, C.K. Cheng, and S.H. Lee, "Partitioning of Opto-electronic interconnect modules," to appear on *Proc. IEEE MCM Conference*, March 1994.

APPENDIX A

S.K. Patra, J. Ma, V.H. Ozguz, and S.H. Lee, "Alignment issues in packaging for free space optical interconnects," *Optical Engineering,* accepted for publication.

Alignment Issues in Packaging for Free Space Optical Interconnects

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Abstract

The addition of optics to electronics in optoelectronic packaging for free-space optical interconnect alters the nature of electrical packaging design methodologies, as well as the complexity of implementation. One such complexity arises from stringent alignment requirement among microlaser, computer generated holographic element and detector. The alignment achieved in the system is a function of assembly tolerance and working environment such as operating temperature. This paper quantitatively analyzes the impact of these constraints on the alignability of the assembly of free-space optical interconnect.

Contents

APPENDIX B

D. Zaleta, S.K. Patra, J. Ma, and S.H. Lee, "Misalignment sensitivity analysis of planar optical interconnect systems", Proc. SPIE, 2153, 1994.

Misalignment sensitivity analysis of planar optical interconnect systems

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ABSTRACT

In order to fabricate practical free-space optical interconnect systems, a thorough understanding of the effect of optical misalignment on the power throughput of an optical link is required. Further, not only assembly tolerances (resulting in misalignment) but also component manufacturing tolerances that also introduce vignetting into the optical system need to be studied. We present a study of assembly and component manufacturing errors and their effect on the integrated power falling onto the detector for planar space variant optical systems. We also show the trends of the different misalignment sensitivities as the interconnect distance increases.

1. INTRODUCTION

The development of optical interconnect systems into practical systems is limited by a number of factors mainly related to packaging. Planar approaches as proposed by Goodman et. al.[1] and Jahns et. al.[2] and transmissive planar approaches as proposed by Iga et. al.[3] are currently the most promising general optical designs for integration with optoelectronics. Problems related to alignment, thermal heat dissipation, and integration of dissimilar materials are just a few of the major factors that these next generation optical interconnect systems must address. In particular, misalignment in the optical interconnect system either due to assembly errors and to component manufacturing errors create new issues in optoelectronic packaging that are not present (at least to the degree required of optics) in electronic packaging. Recently, the alignment issue in optical interconnect systems has received increasing attention by several authors[4,5,6].

In this paper, we attempt to provide a detailed analysis over a wide variety of general misalignments that can occur in general space variant optical interconnects for inter- and intra-MCM systems. To measure the system's sensitivity to misalignment, we will use the integrated power at the detector as our metric, since this is what is of primary interest to the system designer to calculate such system performance parameters as BER and SNR. We will also show that while most of the misalignments have an increased sensitivity for longer interconnect distances some are either unaffected or actually have decreased sensitivity. The eventual goal of this work is to develop general analysis techniques to allow tolerancing of the packaging alignment and component manufacturing so that practical systems can be made as inexpensively as possible. This tolerancing of optical interconnect systems will allow variations from nominal specifications to ensure that a certain power level at the detector is maintained for a statistically significant number of systems. Toward this goal, this paper will present a general method of analysis for determining the sensitivity of a large number of misalignments in planar packaged systems and their effect on the integrated power falling on the detector.

The organization of the paper is as follows. Section 2 will discuss the kinds of and classification of misalignments for a general space variant optical interconnect design. Then Section 3 will discuss the approach taken and Section 4 will discuss the results of the sensitivity analysis and how the sensitivities vary with increasing interconnect distances. Finally, Section 5 will summarize the work and attempt to draw some conclusions and directions for future work from the research thus far performed.

2. TYPES OF MISALIGNMENTS FOR SPACE VARIANT SYSTEMS

Figure 2.1 shows a schematic diagram of the type of space variant system that we are considering and some of the misalignments associated with it. This system is considered to be an optoelectronic MCM (MultiChip Module) system which is made up of several electronic chips that are interconnected optically and placed onto a single MCM substrate, although nothing in this analysis prevents it from also representing communication between MCMs. To make this analysis

APPENDIX C

H. Takahashi, D. Zaleta, J. Ma, J.E. Ford, Y. Fainman, and S.H. Lee, "Packaged optical interconnection system based on photorefractive correlation," *Applied Optics*, accepted for publication.

Packaged optical interconnection system based on photorefractive correlation

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Joseph E. Ford, Yeshaiahu Fainman, and Sing H. Lee

ABSTRACT

We present an experimental implementation of a packaged free-space optical interconnection system by photorefractive correlation. The system consists of a phase code, a $LiNbO_3$ crystal, two CGH Fourier transform lenses, and a detector, all mounted on a glass substrate. Interconnections between 5x5 arrays are demonstrated with an SNR of 10. We also discuss the possibility of applying this packaging method to interconnections between larger arrays.

Key words: Optical interconnects, photorefractive, optical packaging.

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APPENDIX D

J. Ma, B. Catanzaro, W. Daschner, Y. Fainman, and S.H. Lee, "Packaged reconfigurable space-variant optical interconnect using wavelength multiplexed volume holograms," *Proc. SPIE,* **1849**, 116-128(1993)

Packaged reconfigurable space-variant optical interconnect using wavelength multiplexed volume holograms

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ABSTRACT

The packaging opto-electronic interconnects has the potential to create compact, highly dense communication networks. We present a packaged space-variant optical interconnect module using wavelength multiplexed volume holographic elements recorded in photorefractive materials. The input/output arrays (4 x 4), an illumination lenslet array, and a set of two wavelength multiplexed off-axis volume holographic lenslet arrays were integrated with a series of several glass substrates to form a free-space optical interconnect. The size of the packaged optical interconnect module was 40mm x 24mm x 37mm. Reconfigurable interconnection was demonstrated on the packaged module by performing the perfect shuffle and butterfly networks, at different wavelengths. Several packaging issues, such as alignment, bonding, energy efficiency and system scalability were studied.

1. INTRODUCTION

Optical interconnects can be used to remove two important communication bottlenecks: communication between processing elements in a parallel processing array and communication between these processing elements and memories [1]. Reconfigurability is particularly important because it can be used to address such needs as network contention and fault tolerance [2]. Optical reconfiguration can be achieved by wavelength multiplexing several interconnects inside a volume hologram [3,4]. By packaging the optical system, the issues of compactness and ruggedness can be resolved [5], and it provides the opportunities for mass production.

The optical interconnect module packaged was the space-variant system shown in Fig.1. The space-variant design is very flexible: able to perform any arbitrary interconnection pattern, from very regular to highly irregular. In this design, the first holographic optical element (HOE) plane collimates the light from the source and diffracts the beam to the desired location(s). The second HOE focuses the beam onto the detectors. In our design we chose to use photorefractive volume holograms as the HOEs for three reasons. First, volume hologram provides much larger diffraction angle than the electron-beam fabricated computer generated hologram, giving rise to a reduced system size. Second, reconfigurable interconnects can be realized by using wavelength multiplexing. Third, in-situ recording could be used to ease the problem of aligning the holograms during bonding.

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APPENDIX E

D. Zaleta, W. Daschner, M. Larsson, B. Kress, J. Fan, K.S. Urquhart, and S.H. Lee, "Diffractive optics fabricated by electron-beam direct write methods," *Proc. SPIE* Critical Review, CR49, 1993.

Diffractive optics fabricated by electron-beam direct write methods

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ABSTRACT

Due to the stringent requirements on the lateral alignment and the large number of steps required to fabricate diffractive optics by typical microlithographic techniques, the need for more efficient methods to fabricate these elements has arisen. This paper discusses the use of electron beam lithography in fabricating diffractive optical elements by direct e-beam alignment and direct write into the electron beam resist. Many of the practical advantages and disadvantages of each method will be pointed out. In particular, current research and future research directions into such direct write problems as the proximity effect, hologram ruggedness, and lengthy exposure times will be addressed.

1. INTRODUCTION

In order to fabricate high performance diffractive optical elements (DOEs) with reliable quality, it was noted that powerful microlithographic techniques developed for integrated electronic circuits could be utilized[1]. However, these techniques typically have difficulty with misalignment between masking steps and long processing times in order to achieve high efficiency. Due to the advanced alignment and exposure facilities available on an electron beam writer, electron beam methods of aligning patterns and exposing these patterns directly into electron beam resist have been developed. It is this latter technique of actually creating the desired surface relief phase profile into the electron beam resist that has sparked a great deal of current research interest. This technique, generally termed direct write electron beam lithography (EBL), not only drastically reduces the number of processing steps to achieve a given DOE but also results in a more continuous surface profile.

This paper will begin by describing the conventional use of photolithography to fabricate binary optics in the next section. Section 3 will detail some of the electron beam techniques that have been developed to reduce misregistration between multiple patterns while maintaining the high vertical accuracy. Section 4 will discuss in detail the direct write EBL technique, its advantages, and some of its drawbacks. We shall then address some of the drawbacks of this method due to the proximity effect, the ruggedness, and the exposure time inherent in this technique and mention current directions in solving these problems. Finally, in Section 5, a summary of the paper will be given.

APPENDIX F

J. Fan, D. Zaleta, and S.H. Lee, "An algorithm for the generation of reduced E-beam fabrication data for general aspheric diffractive optical elements," submitted to *OSA Topical Meeting on Diffractive Optics*, Rochester(June 1994).

An Algorithm for the Generation of Reduced Ebeam Fabrication Data for General Aspheric Diffractive Optical Elements

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I. Introduction

Diffractive optical elements (DOEs) can be used in many industrial and military applications including optical interconnections for the next-generation highly parallel computing systems. One of the most general DOEs for such applications is the aspheric DOE. Typically an aspheric element is defined as an optical element whose phase function can be specified by a polynomial of some specified type. Thus aspheric elements can be designed in standard optical design programs such as CODEV that will optimize the coefficients of the polynomial to satisfy the designer's specifications. Once these coefficients are generated the problem is to generate the data necessary to fabricate the aspheric DOE. However, current ebeam pattern generators for vector based machines (such as Cambridge) place stringent limitations on the types of shapes that can be generated. For instance only trapezoids with horizontal tops and bottoms and with a fixed set of angles for the trapezoid's sides are allowed. As the number of trapezoids grow, the ebeam data size grows proportionally. Thus, there is a tradeoff in data generation between pattern fidelity and data size or between optical noise and fabrication cost/time. Therefore, there is a need for general algorithms that generate reduced data size for general aspheric DOEs.

Arnold[1] first proposed the use of the ebeam writer in generating DOEs, however only sketchy algorithms were given on how to take specification data such as the coefficients of an aspheric DOE and generate the ebeam data. Later, two general methods were proposed to generate aspheric DOEs: fringe tracing based algorithms that trace fringe boundaries [2], and pixel based algorithms that draw small areas (pixels) based on the average wavefront values[3]. Fringe tracing based algorithms are not stable nor general enough to ensure successful data generation but they produce far less data than pixel based approaches. In this paper, we present a new algorithm based on modified subdivision techniques[4] that possesses the stability of pixel-based approaches but at the same time significantly reduce the amount of data by using fringe tracing.

II. Algorithm

In this section we will formally describe the problem to be solved and present an algorithm capable of providing a general solution to the problem.

A. Problem formulation

Let A be the aperture region of a DOE: $x_0<x<x_1$ and $y_0<y<y_1$.

Let $S=\{E \mid E \text{ is an allowable ebeam shape}\}$ be the allowable ebeam shapes.

Let $P(x,y)$ be a polynomial phase function defined in region A, which represents the desired wavefront of interest. Given the fractional fringe phase value, $2\pi/m$, where m is the number of phase levels, and a phase error bound e. Our problem is to partition A into a set of fringes A_i such that $A_i=\{(x,y) \mid (i-1)\times(2\pi/m)< P(x,y)\le i\times(2\pi/m)\} \quad \forall i.$ (1)

APPENDIX G

D. Zaleta, M. Larsson, W. Daschner, and S.H. Lee, "Coupled kinoforms to increase power throughput for space variant optical interconnect systems," submitted to *OSA Topical Meeting on Diffractive Optics*, Rochester (June 1994).

Coupled Kinoforms for Space Variant Optical Interconnect Systems

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1.0 Introduction

Space variant optical interconnect systems have the benefit of permitting fully random interconnections between input and output optoelectronic devices in two arbitrary located processing elements (PEs) as shown in Figure 1. Due to the fact that diffractive optical elements (DOEs) can support random interconnect patterns, they are attractive to implement space variant types of systems. However, the small apertures (≤1 mm), the limited space bandwidth product, and the high efficiency specifications required of these systems conflict with the desire to maintain large distances (>1 cm) between the input and output optoelectronic devices. The small DOE apertures found in these types of systems make diffraction a dominant consideration. Likewise, the limited space bandwidth product makes it difficult to achieve large angles in folded planar systems. Several papers have addressed techniques to increase the angle by multiple DOEs [1] or by special encoding techniques [2]. However, these angles are still relatively small (<25°) resulting in the need to increase longitudinal distances in order to realize the desired lateral interconnect distance. Thus, there is a need to develop design methods that permit one to maximize the distance traversed by the interconnect while maintaining as high efficiency as possible. In this paper, the authors present three methods utilizing the Gerchberg-Saxton (GS) [3] algorithm to design coupled kinoforms that are capable of maximizing the optical power on the detector while maintaining diffraction-limited distances for many types of space variant systems. These designs are compared to a "standard" space variant design.

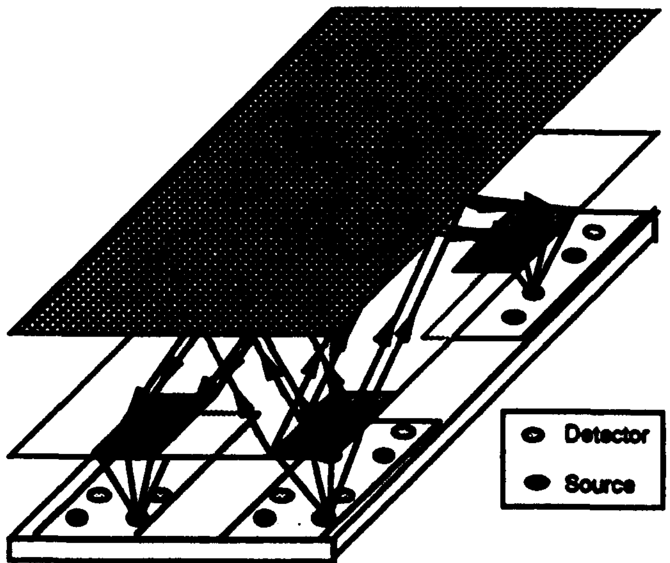

Figure 1. Schematic diagram of space variant optical interconnect system.

2.0 Standard Space Variant Optical Design

Our goal in this paper is to increase the lateral interconnect distance in a planar space variant optical system by increasing the propagating distance between the two elements to some diffraction limited level that permits the maximum optical throughput. Figure 2 shows a modified optical interconnect that was recently proposed for achieving diffraction limited performance in space variant optical systems[4]. In this system, we wish to transfer as much light as possible to the opposite side by forcing the focal length of DOE #1 (Fresnel lens) to be

APPENDIX H

S.H. Lee, V.H. Ozguz, J. Fan, D. Zaleta, and C.K. Cheng, "Computer aided design and packaging optoelectronic systems with free space optical interconnects", *Proceedings of IEEE 1993 Custom Integrated Circuits Conference*, May 9-12, 29.3.1-29.3.41993.

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COMPUTER AIDED DESIGN AND PACKAGING OPTOELECTRONIC SYSTEMS WITH FREE SPACE OPTICAL INTERCONNECTS

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ABSTRACT

This paper provides an introduction to current research in computer aided design and packaging for optoelectronic systems utilizing free space optical interconnects. New computer aided design tools will be presented that allow layout of multistage networks based upon CGH fabrication limitations and the subsequent synthesis of the interconnect holograms. Recent work involving double-sided alignment of a single substrate as well as alignment techniques between two different substrates will be discussed. We will also present several packaged systems utilizing photorefractive crystals to minimize alignment problems.

1. INTRODUCTION

Optoelectronic computing systems connected by free space optical interconnects are comprised of electronic elements (processors, logic circuits), optoelectronic elements (modulators, detectors, light sources) and optical elements (diffractive and refractive lenses, polarizers, beam splitters etc.). Optical interconnects are incorporated to aid electronics in overcoming some of their interconnection problems. However, the addition of optical and optoelectronic elements to electronic elements increases the complexity of the design and packaging tasks. Therefore, new CAD tools are required allowing the combination of optics, optoelectronics, and electronics based on optical/optoelectronic technology constraints. Section 2 will present recent work on developing layout and synthesis tools based on the unique needs of optoelectronic systems. Packaging techniques also need to be developed to assemble these elements in a compact, rugged, reliable and manufacturable way. There are many packaging issues that are common between electronic and optoelectronic systems, such as area or volume, material compatibility, thermal management, testing, modularization/connectorization and signal integrity analysis. However, there are also new packaging issues, such as alignment between the optical and electronic parts of the system that need to be addressed. Section 3 will discuss several optical alignment and packaging efforts recently accomplished.

2. OPTOELECTRONIC COMPUTER-AIDED DESIGN

New computer-aided tools are needed for the development of OptoElectronic MultiChip Modules (OE-MCMs) utilizing free-space optical interconnects. In the electronic world, one of the challenges in designing large systems is the physical placement and routing of electronic modules based on the system's physical and performance constraints. Unfortunately, the standard algorithms used by electronics fail to properly model optoelectronic constraints. For instance, they minimize a cost function that incorporates the sum of all the interconnection distances and allow for a configuration space that permits the modules being placed to overlap. In the optoelectronic case, it has been shown[1] that for free-space optical interconnection for OE-MCMs, it is the maximum interconnection distance that should be

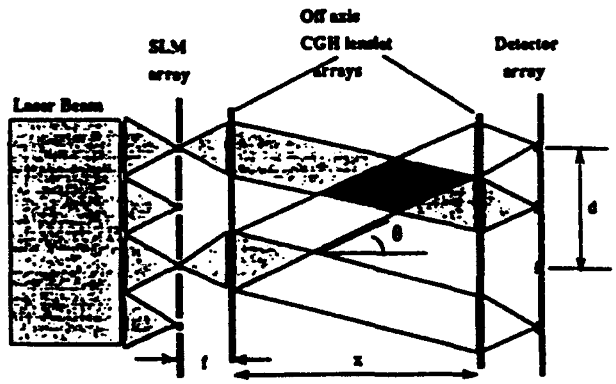

Figure 1. Optical interconnect configuration

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APPENDIX I

D.-T. Lu, W.P. Poon, T.-T.Y. Lin, and S.H. Lee, "Optoelectronic component modeling and system simulation," *1993 OSA Annual Meeting*, Toronto(October 1993).

matched with the LP_{11} mode of the output fiber at the wavelength of operation. Power coupling thus takes place between these two modes. Spectral characteristics of the proposed filter are analyzed using coupled-mode theory. Numerical results are presented for example cases corresponding to peak transmission at 1330 nm and 1550 nm wavelengths. 3-dB spectral widths less than 1 nm have been predicted. The narrow spectral width is due to a large difference between the slopes of the dispersion characteristics of the two interacting modes in the coupling region. The effect of core separation on the spectral width is also examined. The application of this device in wavelength division multiplexing and for mode conversion purposes is addressed.

MGG5 2:30 pm

Coupled-waveguide Fabry–Perot spectral filter, A. Safaai-Jazi, C.C. Chang, *Bradley Department of Electrical Engineering, Virginia Polytechnic Institute and State University Blacksburg, Virginia 24061-0111. e-mail: JAZI@VTVM1.cc.vt.edu.* A novel coupled-waveguide Fabry–Perot structure is proposed and studied using coupled-node theory. The proposed structure consists of two coupled parallel optical waveguides with partially reflecting mirrors at both ends. Two mechanisms contribute to the operation of the device: (1) interference of counter propagating waves resulting from reflection by end mirrors; (2) evanescent field coupling between the parallel waveguides. Thus, the proposed device exhibits the attributes of both Fabry-Perot resonator and the directional coupler. Spectral characteristics of the device are calculated using a coupled-mode theory based on mode partition approach. The constituent waveguides may be identical or unidentical. The advantage of the unidentical waveguide structure is the phase mismatch between the two guides and hence non-periodic transmission characteristics. Numerical results for several example cases are presented. The results indicate that significant improvement in mode discrimination capability and longitudinal mode spacing over the conventional Fabry-Perot resonator is achieved. Applications of the proposed device in single-frequency diode lasers and in wavelength division multiplexing are addressed.

MGG6 2:45 pm

Modeling and simulation of ARROW couplings, C. L. Xu*, W. P. Huang*, C. Barnard, J. Chrostowski, S. T. Chu**, *National Research Council of Canada, Institute for Information Technology, Ottawa, Ontario, Canada K1A 0R6.* The characteristics, such as the propagation constant and the propagation loss, of an isolated ARROW have been studied and are well understood[1,2]. On the other hand, more research is needed for coupled-ARROWs, which have great potential for optical interconnects[3], wavelength filters[4], and optical switching. For those coupled-ARROWs, the cross-coupling should be well controlled. The BPM, which can trace the wave propagation, is a more rigorous method than the conventional transverse resonant method (TRM) used to study the ARROW. Unlike TRM, which is only limited to 2-D structures, BPM can simulate both 2-D and 3-D structures.

Since an ARROW has a larger core size than a conventional waveguide the input coupling to an ARROW is expected to be much more efficient. However, when an optical beam is coupled to an ARROW reflection and radiation are occur due to the mismatch between the input field and the mode profile of the ARROW structure. The coupling efficiency depends on the relative position of the input beam and the waveguide. Also, as the coupling alignment changes, different modes with different propagation constants and different propagation losses may be excited. Hence, the ARROW guiding characteristics are also input sensitive. All of these effects can be investigated by BPM and FDTD. Specific examples will be presented at the conference.

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**Yokohama National University, Division of Electrical and Computer Engineering, Yokohama, Knagawa 240, Japan.

MGG7 3:00 pm

Optoelectronic component modeling and system simulation, Dau-Tsuong Lu, Wang P. Poon, Ting-Ting Y. Lin, Sing H. Lee, *University of California, San Diego, Department of Electrical and Computer Engineering, 9500 Gilman Drive, La Jolla, CA 92093-0407. E-mail: lu@ece.ucsd.edu.* Detailed system simulation before actual construction helps designers to verify system design under normal or adverse operating environments. For computing systems, a good simulator can also facilitate early algorithm and software development. The models needed to verify system performance at 5 degrees Celsius have different requirements than those needed for software development. We are developing models for optoelectronic components: sources/modulators, detectors, refractive and diffractive optical elements. These behavioral models are created and managed using tools from Mentor Graphics. The same libraries will also contain estimation models and geometrical models for physical design automation. These models allow system designers to construct a system by connecting models together through a graphical user interface. The designer can then select the level of physical details desired for simulation. We will illustrate how this software tool can be used to predict the signal integrity of optical interconnects in an optoelectronic system.

MHH 1:30 pm
104C

Nonlinear Materials and Measurement

Presider to be announced

MHH1 1:30 pm

Z-scan technique using top-hat beams, W. Zhao, P. Palffy-Muhoray, *Liquid Crystal Institute, Kent State University. Kent, Ohio 44242. zhao@scorpio.kent.edu.* The Z-scan technique developed by Sheik-Bahae[1] is straightforward method of accurately measuring intensity dependent optical nonlinearities of materials. It is based on self-focusing or defocusing of an optical beam by a thin sample. To date, primarily Gaussian beams have been used in Z-scan measurements; however, Gaussian beams are not always readily available. Beams with top-hat profiles are more readily obtained. Comparing the results of measurements using Gaussian and top-hat beams provides an estimate of the dependence of Z-scan results on beam profile. For the case where the sample has no nonlinear absorption, we give a simple analytic expression relating the normalized transmittance and the

APPENDIX J

D. Zaleta, J. Fan, B.C. Kress, S.H. Lee, and C.K. Cheng, "Optimum placement for optoelectronic multichip modules and synthesis of diffractive optics for MCM interconnects," *Applied Optics*, accepted for publication.

Optimum Placement for Optoelectronic MultiChip Modules and the Synthesis of Diffractive Optics for MCM Interconnects

David Zaleta, Jiao Fan, Bernard C. Kress, Sing H. Lee, Chung-Kuan Cheng

Decreasing the system volume for optoelectronic planar systems is achieved by advancing computer-aided design of OptoElectronic MultiChip Modules (OE MCM). It is shown that in order to minimize the volume in OE MCM, it is necessary is to minimize the maximum interconnect distance. To achieve this, we have developed placement algorithms based on the constraints of a given irregular interconnect pattern. Results are given for a twin butterfly network for two general physical models: transmissive MCM and reflective MCM. We then show three different types of hologram designs that can be used to implement the interconnect array. These elements are for reconstruction in the near field and are fabricated by direct write electron beam lithography. Both simulated and experimental reconstructions are demonstrated.

Key Words: Optoelectronic CAD, Placement, Optoelectronic MCM, Diffractive Optics, Optical Interconnects.

1. Introduction and Background

In order for optical technologies to be incorporated into the next-generation parallel computers, new optoelectronic computer-aided design, integration and packaging technologies must be investigated. Current work has been primarily directed toward integrating optoelectronic and electronic technologies[1-3] and packaging of optical elements such as diffractive (or binary) optics into compact configurations[4-6]. One of the main issues in the packaging area is the

APPENDIX K

J. Fan, B. Catanzaro, V.H. Ozguz, C.K. Cheng, and S.H. Lee, "Design considerations and algorithms for partitioning opto-electronic multichip modules," *The First International Workshop on Massive parallel Processing using Optical Interconnections.* Cancun Mexico, April, 1994.

Design Considerations and Algorithms for Partitioning Opto-Electronic Multichip Modules

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ABSTRACT

There is considerable interest in developing optical interconnects for multi-chip modules (MCM). As a consequence, there is the basic need in developing a methodology for partitioning the system for effective utilization of the optical and electronic technologies. For the given netlist of a system design, key question to be answered is where to use optical interconnections. This paper introduces the Computer Aided Design (CAD) approach for partitioning opto-electronic systems into Opto-Electronic Multichip Modules (OE MCM). We will first discuss the design tradeoff issues in optoelectronic system design including speed, power dissipation, area and diffraction limits for free space optics. We will then define a formulation for OE MCM partitioning and describe new algorithms for optimizing this partitioning based on the minimization of the power dissipation. The models for the algorithms are discussed in detail and an example of a multistage interconnect network is given. Different results, with the number and size of chips being variable, are presented where improvement for the system packaging has been observed when the partitioning algorithms are applied.

1. INTRODUCTION

Opto-electronic interconnection has been proposed as a technology that can be used to increase the throughput and the total bandwidth of interconnection in high performance computing and communication systems[1]. Optical interconnection provides speed advantage over electrical interconnection in large systems. Routing information in 3D space, free space optical interconnection offer higher connectivity than fiber or waveguide. Electronic and optical interconnects have been compared at device level and a break-even line length has been defined[2]. For interconnects longer than this line length, optics is the preferred technology for interconnection. The problem, however, is that the logical netlist of a system design does not specify the physical line lengths of the interconnects. The line lengths can only be determined after the design steps of placement and route being completed. Previous studies [3, 4] have tried to answer the question of what system configuration is better by examining specific architectures and networks. Based on the results of the evaluations the system parameters are determined. For